Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027B	Serial No.: ~~Unassigned~~ 10/814866
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: Herewith 3/30/04	Group: Unassigned 2816

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	5,761,121	6/2/1998	Chang	365	185.14	10/31/1996
TH	B	5,825,063	10/20/1998	Diorio et al.	257	316	7/26/1996
TH	C	5,875,126	2/23/1999	Minch et al.	365	185.01	9/26/1996
TH	D	5,898,613	4/27/1999	Diorio et al.	365	185.03	6/25/1997
TH	E	5,914,894	6/22/1999	Diorio et al.	365	185.03	6/1/1998
TH	F	5,986,927	11/16/1999	Minch et al.	365	185.01	11/10/1998
TH	G	5,990,512	11/23/1999	Diorio et al.	257	314	4/22/1997
TH	H	6,125,053	9/26/2000	Diorio et al.	365	185.03	11/30/1998
TH	I	6,144,581	11/7/2000	Diorio et al.	365	185.03	11/30/1998
TH	J	6,222,765	4/24/2001	Nojima	365	185.08	2/18/2000
TH	K	6,452,835	9/17/2002	Diorio et al.	365	185.03	10/27/2000
TH	L	6,477,103	11/5/2002	Nguyen et al.	365	225.7	9/21/2001
TH	M	6,661,278	12/9/2003	Gilliland	327	536	7/8/2002
TH	N	6,664,909	12/16/2003	Hyde et al.	341	144	8/13/2001

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

TH	O	Raszka, Jaroslav, et al., "Embedded Flash Memory for Security Applications in a 0.13μm CMOS Logic Process", IEEE 2004 International Solid-State Circuits Conference, February 16, 2004, pp. 46-47.

Examiner	Date Considered 1/23/06

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

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U.S. Patent Documents

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TH	P	2003/0206437	11/6/2003	Diorio et al.	365	185.03	7/9/2002
TH	Q	2004/0004861	1/8/2004	Srinivas et al.	365	185.21	7/5/2002
TH	R	2004/002/1166	2/5/2004	Hyde et al.	257	314	1/31/2003
TH	S	2004/0037127	2/26/2004	Lindhorst et al.	365	202	5/12/2003
TH	T	2004/0052113	3/18/2004	Diorio et al.	365	185.21	9/16/2002

Foreign Documents

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Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner	Date Considered 1/23/06

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Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027B	Serial No. 10/814,866
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: March 30, 2004	Group: 2818

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	6,320,788	11/20/2001	Sansbury et al.	365	185.1	9/11/00

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

TH	B	Carley, L. Richard, "Trimming Analog Circuits Using Floating-Gate Analog MOS Memory", IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1569-1575, December 1989.
TH	C	Partial International Search for International Application No. PCT/US03/31792, date mailed April 2, 2004.

Examiner	Date Considered
	11/28/06

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027B	Serial No. 10/814,866
Information Disclosure Statement by Applicant (Use several sheets if necessary)	Applicant: Christopher J. Diorio et al.	
	Filed: March 30, 2004	Group: 2818

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	4,571,704	2/18/1986	Bohac, Jr.	365	156	02/17/84
TH	B	5,323,066	6/21/1994	Feddeler et al.	327	143	6/01/92
TH	C	5,892,712	4/6/1999	Hirose et al.	365	185.07	04/29/97
TH	D	6,111,785	8/29/2000	Hirano	365	185.09	08/23/99
TH	E	6,741,500	5/25/2004	DeShazo et al.	365	185.28	10/04/02

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
TH	F	0 326 883	8/9/1989	EP			X	
TH	G	0 336 500	3/30/1989	EP			X	
TH	H	0 756 379	1/29/1997	EP			X	

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

TH	I	International Search Report for International Application No. PCT/US05/10434, date of mailing 9/13/05.
TH	J	International Search Report for International Application No. PCT/US2005/010432, date of mailing 9/27/05.
TH	K	International Search Report for International Application No. PCT/US2005/010431, date of mailing 9/27/05.

Examiner	Date Considered
	1/26/05

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Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027B	Serial No. 10/814,866
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: March 30, 2004	Group: ~~2818~~ 2816

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	2003/0206437	11/6/2003	Diorio et al.	365	185.21	9/16/02
TH	B	2004/0004861	1/5/2004	Srinivas et al.	365	185.21	7/5/02
TH	C	2004/0021166	2/5/2004	Hyde et al.	257	314	1/31/03
TH	D	2004/0037127	2/26/2004	Lindhorst et al.	365	202	5/12/03
TH	E	2004/0052113	3/18/2004	Diorio et al.	365	185.21	9/16/02
TH	F	5,736,764	4/17/1998	Chang	365	185.14	10/31/96
TH	G	5,777,926	7/7/1998	Trinh et al.	365	185.19	10/24/96
TH	H	5,801,994	9/1/1998	Chang et al.	365	185.29	8/15/97
TH	I	5,841,165	11/24/1998	Chang et al.	257	318	12/22/95
TH	J	5,901,084	5/4/1999	Ohnakado	365	185.18	11/23/97
TH	K	5,912,842	6/15/1999	Chang et al.	365	185.11	10/9/97
TH	L	5,966,329	10/12/1999	Hsu et al.	365	185.18	10/9/97
TH	M	5,982,669	11/6/1999	Kalnitsky et al.	365	185.28	11/04/98
TH	N	6,055,185	4/25/2000	Kalnitsky et al.	365	185.18	0 11/98
TH	O	6,137,723	10/24/2000	Bergemont et al.	365	185.18	04/28/99
TH	P	6,384,451	5/7/2002	Caywood	257	321	3/9/00

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Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

TH	Q	Invitation to Pay Additional Fees (Partial International Search), Application No. PCT/US 03/31792, date of mailing April 22, 2004.
TH	R	Witters, et al., "Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits", IEEE Journal of Solid-State Circuits, VOL. 24, No. 5, October 1989, pp. 1372-1380.

Examiner [signature] Date Considered 1/23/06

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.

Form PTO 1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. IMPJ-0027B	Serial No. 10/814,866
Information Disclosure Statement by Applicant	Applicant: Christopher J. Diorio et al.	
(Use several sheets if necessary)	Filed: March 30, 2004	Group: 2818

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
TH	A	4,158,239	1/12/1979	Bertin	365	182	12/20/77
TH	B	4,541,073	9/10/1985	Brice et al.	365	156	9/28/82
TH	C	4,758,869	7/19/1988	Eitan et al.	357	23.5	8/29/86
TH	D	4,935,702	6/19/1990	Mead et al.	330	9	12/9/88
TH	E	5,018,102	5/21/1991	Houston	365	95	12/20/88
TH	F	5,068,622	11/26/1991	Mead et al.	330	253	02/28/90
TH	G	5,438,542	8/1/1995	Atsumi et al.	365	182	10/31/94
TH	H	6,141,247	10/31/2000	Roohparvar et al.	365	185.08	12/21/98
TH	I	6,214,666	4/10/2001	Mehta	438	257	12/18/98
TH	J	6,363,006	3/26/2002	Naffziger et al.	365	154	3/19/01
TH	K	6,363,011	3/26/2002	Hirose et al.	365	185.07	7/25/00
TH	L	6,456,992	9/24/2002	Shibata et al.	706	33	03/25/96
TH	M	6,469,930	10/22/2002	Murray	365	185.08	12/30/00
TH	N	6,573,765	6/3/2003	Bales et al.	327	108	12/30/01
TH	O	6,633,188	10/14/2003	Jia et al.	327	217	02/12/99
TH	P	6,845,029	1/18/2005	Santin et al.	365	96	08/18/04
TH	Q	6,946,892	9/20/2005	Mitarashi	327	333	01/62/04

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

TH	R	Declercq et al., "Design and Optimization of High-Voltage CMOS Devices Compatible With a Standard 5 V CMOS Technology", IEEE Custom Integrated Circuits Conference, 1993, pp. 24.6.1-24.6.4.
TH	S	Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique", IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 374-378.
TH	T	International Search Report for PCT/US 03/31792 date mailed August 12, 2004.

Examiner	Date Considered
	02/02/06

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